From the
INTERNATIONAL SEARCHING AUTHORITY

PCT

To:
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WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing (*day/month/year*)	1 0 MAR 2005

Applicant's or agent's file reference	FOR FURTHER ACTION
9138-0148	See paragraph 2 below

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/US04/03609	05 February 2004 (05.02.2004)	05 February 2003 (05.02.2003)

International Patent Classification (IPC) or both national classification and IPC

IPC(7): G06F 9/45, 17/50 and US Cl.: 717/151, 154-158; 716/2, 7, 17

Applicant

ARIZONA BOARD OF REGENTS

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1. This opinion contains indications relating to the following items:

☒ Box No. I Basis of the opinion

☐ Box No. II Priority

☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

☐ Box No. IV Lack of unity of invention

☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

☐ Box No. VI Certain documents cited

☒ Box No. VII Certain defects in the international application

☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/ US	Authorized officer *Michelle R. Esson*
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450	Kakali Chaki
Facsimile No. (703)305-3230	Telephone No. (703)305-3900

Form PCT/ISA/237 (cover sheet) (January 2004)

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the origina! language into the following language _____, which is the language of a translation furnished for the purposes of internationai search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material

   ☐ in written format

   ☐ in computer readable form

   c. time of filing/furnishing

   ☐ contained in international application as filed.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

Form PCT/ISA/237(Box No. I) (January 2004)

Box No. V Reasoned statement under Rule 43 *bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	NONE	YES
	Claims	1-11	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-11	NO
Industrial applicability (IA)	Claims	1-11	YES
	Claims	NONE	NO

2. Citations and explanations:

Please See Continuation Sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

Claim 11 is objected to under PCT Rule 66.2(a)(iii) as containing the following defect(s) in the form or contents thereof: lines three contains "b" instead of "by".

| Box No. VIII | Certain observations on the international application |

The following observations on the clarity of the claims, description, and drawings or on the questions whether the claims are fully supported by the description, are made:

Claim 11 is objected to under PCT Rule 66.2(a)(v) as lacking clarity under PCT Article 6 because claim 11 indefinite for the following reason(s): last claim in list of claims labeled 1 where it should be claim 11.

Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

V. 2. Citations and Explanations:

Claims 1-11 lack novelty under PCT Article 33(2) as being anticipated by Janssen et al., "A Specification Invariant Technique for Regularity Improvement between Flow-Graph Clusters*".

Claim 1

Janssen disclosed a method of fabricating a reconfigurable processor for running moderately complex programming applications comprising:

(a) providing source code for a programming application *(page 138, section 1)*,

(b) entering the source code in a control flow graph generating compiler to produce a control data flow graph control flow and branch points *(page 141, section 4.4)*,

(c) extracting form the control flow graph basic blocks of code lying between branch points *(page 141, figures 4 and 5)*,

(d) from the code lying between the branch points generating intermediate data flow graphs *(page 141, section 4.4)*,

(e) identifying clusters shared among dfgs at the highest level of granularity *(page 140, section 4)*,

(f) from the identified clusters determining the largest common subgraph shared among the dfgs *(page 140, section 140, shFG)*,

(g) scheduling the largest common subgraph for fast accomplishment of operation in the lcsg *(page 142, figure 6)*,

(h) apply the scheduled lcsg to the intermediate flow graphs replacing the unscheduled lcsg therein *(page 141, section 4.4)*,

(i) scheduling the intermediate flow graphs containing the lcsg's for fast accomplishment of operations in the intermediate flow graphs to derive data patches having operations and timings of each intermediate flow graph *(page 141, section 4.4)*,

(j) combing the data patches to include operations and timing of the lcsg with operations and timings of each intermediate subgraph that are outside the lcsg *(page 142, left column, top)*,

(k) from the combined data patches scheduling for process time reduction multiple uses of the lcsg operations and timings necessary to accomplish operations and timings of all intermediate subgraph employing the lcsg *(page 142, left column)*, and

(l) implementing in hardware having mixed granularities the operations and timing of the lcsg incluging:

      (i) partitioning,

      (ii) placing, and

      (iii) interconnection routing *(page 138, section 1 ; page 140, section 4.1)*.

Claim 2

Janssen disclosed in a method of making an integrated circuit for use as a hardware implemented part of a programmed operation implemented in software and hardware *(abstract)*; the improvement comprising identifying hardware circuit elements for execution of a largest common subgraph common among a set of flow graphs representing the programmed operation *(page 140, section 4)*; partitioning into blocks the circuit elements *(page 139, figure 2)*; arranging the blocks on an area representative of an available area of a surface of a substrate on which the circuit elements are to be formed *(page 139, figure 2)*; routing interconnections among the blocks; partitioning into sub-blocks the circuit elements of each block; arranging each sub-block on an area representative of the block

Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

form which it has been partitioned routing interconnections among the sub-blocks and iteratively partitioning and routing among lesser sub-blocks until the individual circuit elements have been placed and routed *(page 140, element 3)*.

Claim 3

Janssen disclosed the method according to claim 2, wherein the steps of routing comprise locating conductors and switches for interconnections among blocks, sub-blocks and circuit elements *(page 140, section 4.1)*.

Claim 4

Janssen disclosed the method according to claim 3, wherein locating conductors and switches further comprises locating variable switches to effect variable conductive paths among the blocks, sub-blocks and circuit elements *(page 140, section 4.1)*.

Claim 5

Janssen disclosed a method of scheduling process elements of hardware implementing a software application, comprising:
(a) developing a control data flow graph from the software *(page 140, section 4 and 4.1)*;
(b) using a first, non-exhaustive scheduling algorithm to relatively quickly arrive at a first scheduling of the process elements *(page 140, section 4)*;
(c) using a second more exhaustive scheduling algorithm for at least one and less than all selected paths of the control data flow graph to reduce the time of execution thereof *(page 140, section 4)*; and
(d) once all paths of the control data flow graph have been scheduled, including all of the second more exhaustive scheduling, merge all of the schedules, respecting data and resource dependencies *(page 140, section 4 and figure 3)*.

Claim 6

Janssen disclosed the method of scheduling according to claim 5, wherein step (a) comprises PCP scheduling *(page 140, section 4.1)*.

Claim 7

Janssen disclosed the method of scheduling according to either claim 5 or 6, wherein step (b) comprises branch and bound based scheduling *(Abstract; page 140, section 4)*.

Claim 8
Janssen disclosed a dedicated integrated circuit for performing the software operation having processing elements scheduled according to claim 5 *(page 138, section 1)*.

Claim 9
Janssen disclosed a dedicated integrated circuit for performing the software operation having processing elements scheduled according to claim 6 *(page 138, section 1)*.

Claim 10
Janssen disclosed a dedicated integrated circuit for performing the software operation having processing elements scheduled according to claim 7 *(page 138, section 1)*.

Claim [11]
Janssen disclosed the method of forming an application specific reconfigurable circuit, comprising:
(a) providing source code for an application to be run b[y] the circuit *(Abstract)*,
(b) deriving flow graphs representing separate portions of the application *(page 139, figure 2; page 140, section 4)*,
(c) identifying at least one largest common flow graph from at least two of the separate portions of the application *(page 140, section 4, shFG)*; and
(d) configuring in hardware circuitry to be shared by the separate portions of the application *(page 138, section 1; page 140, section 4)*.

Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

Claims 1-11 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.